Please replace Claims 39 - 41 with the following like numbered claims:

39. (Twice Amended) A method according to Claim 35:

wherein the step of forming the dielectric layer comprises the step of forming the dielectric layer on an integrated circuit substrate, the dielectric layer including the closed via and an open via therein; and

wherein the step of forming the conductive pattern comprises the step of forming the conductive pattern in the closed via, in the open via and on the dielectric layer opposite the substrate.

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40. (Twice Amended) A method of forming a bonding pad for an integrated circuit comprising the steps of:

forming a dielectric layer having first and second opposing faces on an integrated circuit substrate, the dielectric layer including a closed via therein that extends from the first face to the second face and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer, wherein the closed via penetrates through the dielectric layer and extends towards the integrated circuit substrate; and

forming a conductive pattern that extends from the first face to the second face in the closed via and on the dielectric layer opposite the substrate.

41. (Amended) A method according to Claim 40 wherein the step of forming the conductive pattern comprises forming the conductive pattern in the closed via and on the dielectric layer opposite the substrate, wherein the conductive pattern penetrates through the dielectric layer and extends towards the integrated circuit substrate.

Please add the following new Claim 42:

42. (New) A method according to Claim 35 wherein the dielectric layer comprises a first dielectric layer and the conductive pattern comprises a first conductive pattern and the closed via comprises a first closed via, the method further comprising:

forming a second dielectric layer having first and second opposing faces on the first conductive pattern, the second dielectric layer including a second closed via therein that extends from the first face of the second dielectric layer to the second face of the dielectric layer and that encloses an inner portion of the second dielectric layer, and is enclosed by an outer portion of the second dielectric layer; and then

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forming a second conductive pattern on the second dielectric layer that extends from the first face of the second dielectric layer to the second face of the second dielectric layer in the second closed via and on the second dielectric layer opposite the substrate to form a multilayer bonding pad on the integrated circuit substrate.